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Complete If Known	
Application Number	
Filing Date	
First Named Inventor	Luigi Colombo
Group Art Unit	
Examiner Name	
Attorney Docket No.	TI-36145

Sheet 1 of 2

U.S. PATENT DOCUMENTS

Exam. Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
WL	AA	4,628,588		McDavid	12/16/1986	Entire Document
WL	AB	4,641,417		McDavid	02/10/1987	Entire Document
WL	AC	4,672,419		McDavid	06/09/1987	Entire Document
WL	AD	4,954,867		Hosaka	09/04/1990	Entire Document
WL	AF	5,633,522		Dorleans et al.	05/27/1997	Entire Document
WL	AG	5,723,893		Yu et al.	03/03/1998	Entire Document
WL	AH	5,937,315		Xiang et al.	08/10/1999	Entire Document
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FOREIGN PATENT DOCUMENTS

Exam. Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[5]
	BA							
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OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Exam. Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
WL	CA	"An Investigation of Molybdenum Gate for Submicrometer CMOS", ROBERT F. KWASNICK, EDMUND B. KAMINSKY, PAUL A. FRANK, GERHARD A FRANZ, KENNETH J. POLASKO, RICHARD J. SAIA and THOMAS B. GORCZYA, IEEE Transactions on Electron Devices, Vol. 35, No. 9, September, 1988, pp. 1432-1438.	
WL	CB	"FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering", YANG-KYU CHOI, LELAND CHANG, PUSHKAR RANADE, JEONG-SOO LEE, DAEWON HA, SRIRAM BALASUBRAMANIAN, ADITYA AGARWAL, MIKE AMEEN, TSU-JAE KING and JEFFREY BOKOR, IEEE, 2002, 4 pgs.	
WL	CC	"Silicon Processing for the VLSI Era, Volume 2: Process Integration", STANLEY WOLD Ph.D., Copyright 1990, Lattice Press, 7 pgs.	
WL	CD	"Electrical Characteristics of TiB_2 for ULSI Applications", CHANG SIK CHOI, QINGFENG WANT, CARLTON M. OSBURN, GARY A. RUGGLES and AYAN S. SHAH, IEEE Transactions on Electron Devices, Vol. 39, No. 10, October, 1992, pp. 2341-2345.	
WL	CE	"Mo_2N/Mo GAFF MOSFETs", NANJIN J. KIM and DALE M. BROWN, IEEE, 1982, 4 pgs.	

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UL	CF	"Application of $MoSi_2$ to the Double-Level Interconnections of I^2L Circuits", YOSHITAKA SASAKI, OSAMU OZAZA and SHUICHI KAMEYAMA, IEEE Transactions on Electron Devices, Vol. ED-27, No. 8, August, 1980, 5 pgs.	
WL	CG	"Work Function Controlled Silicide Technology for Submicron CMOS", MASAKAZU KAKUMU and KAZUHIKO HASHIMOTO, No Source or Date Available, pp. 30-31.	
WL	CH	"Refractory Metal Silicide/N+ Polysilicon in CMOS/SOS", B.C. LEUNG and J.S. MAA, No Source or Date Available, pp. 827-830.	
WL	CI	"Fabrication of Mo-Gate/Ti-Silicide-Clad-Moat MOS Devices by Use of Multilayer-Glass Depositions", J.M. McDAVID, IEEE Electron Device Letters, Vol. EDL-5, No. 9, September, 1984, pp. 374-375.	
WL	CJ	"Lightly Impurity Doped (LD) Mo Silicide Gate Technology", MASAKAZU KAKUMU and JUN'ICHI MATSUNAGA, IEEE, 1985, 4 pgs.	
	CK		
	CL		
	CM		
	CN		
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Examiner Signature		Date Considered	1/19/2005

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